EE105
Microelectronic Devices and Circuits:
MOS Large Signal Model and Bias Circuits

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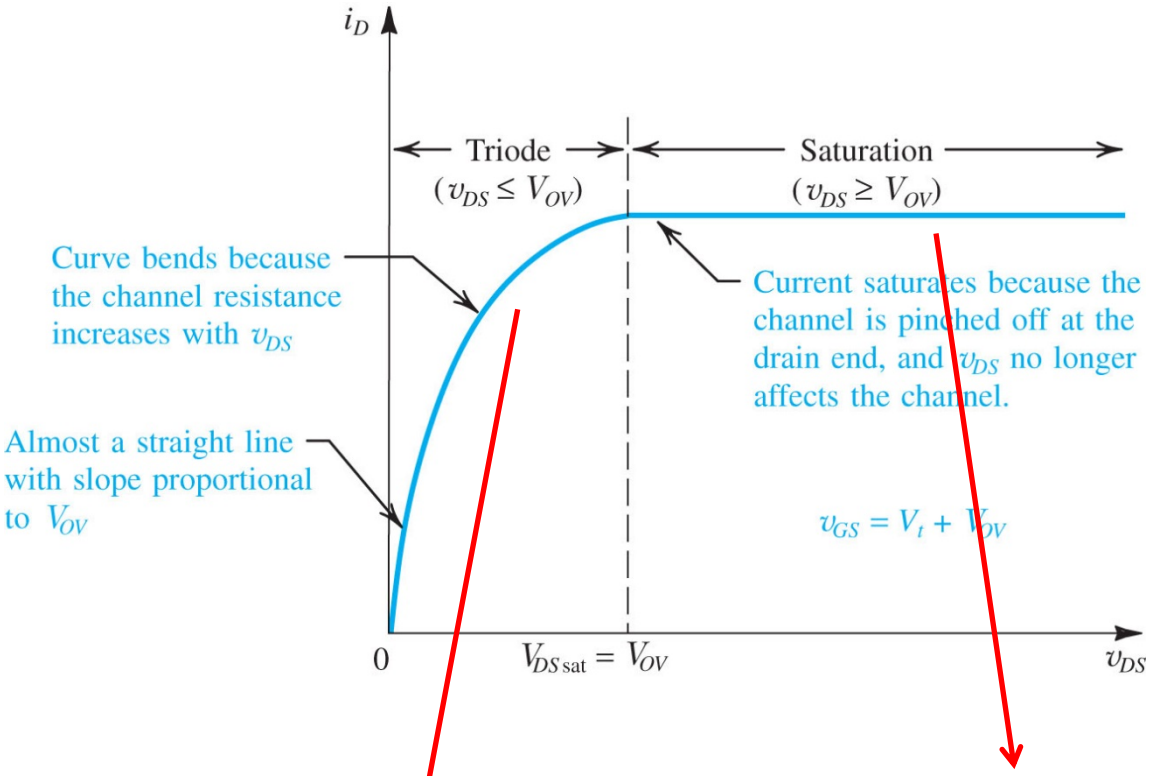
Saturation Region ($v_{DS} > v_{OV}$)



When $0 \le v_{DS} \le v_{OV}$

$$i_D = \mu_n C_{ox} \frac{W}{L}\left(v_{OV} v_{DS} - \frac{1}{2} v_{DS}^2\right)$$

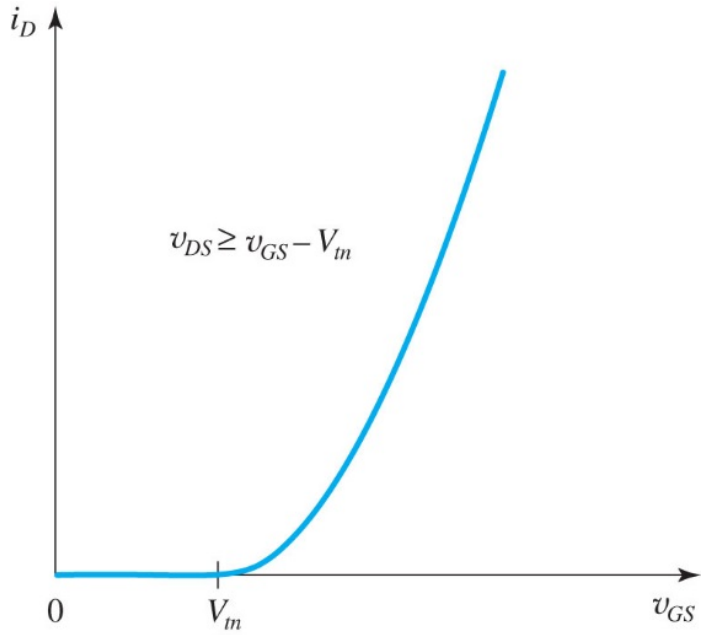
This is called the "Triode Region"

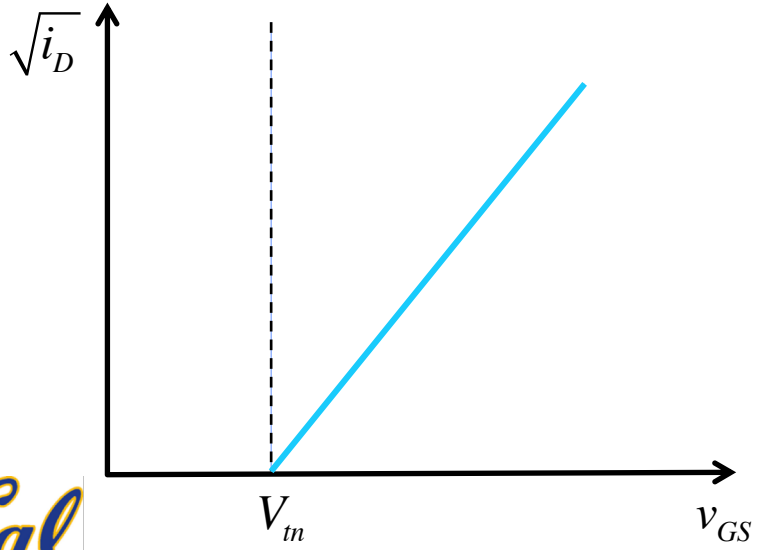
When $v_{DS} > v_{OV}$,

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} v_{OV}^2$$

This is called "Saturation Region"

Drain Current vs Gate Voltage





In Saturation Region

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}v_{OV}^2$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(v_{GS} - V_{tn}\right)^2$$

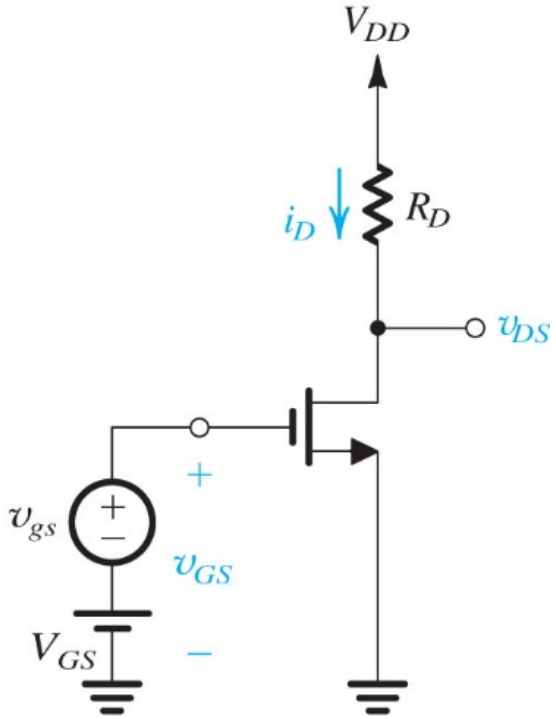
To experimentally determine V_{tn} :

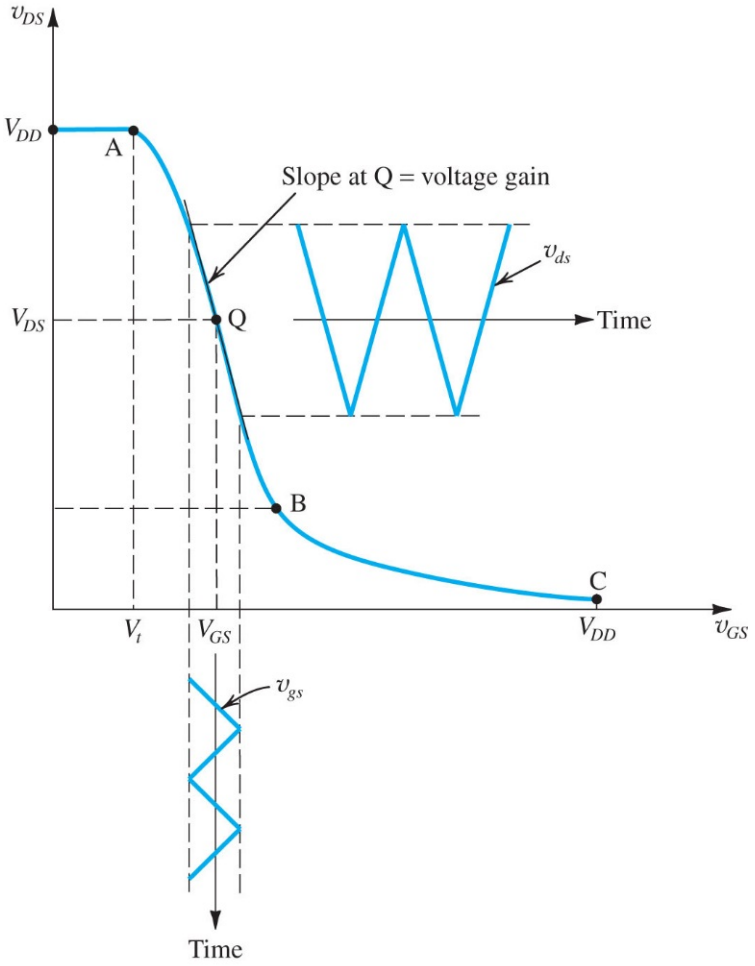
Measure and plot $\sqrt{i_D}$ versus v_{GS}

$$\sqrt{i_D} = \sqrt{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}}\left(v_{GS} - V_{tn}\right)$$

V_{tn} = intercept with horizontal axis

Analog Voltage Amplifier



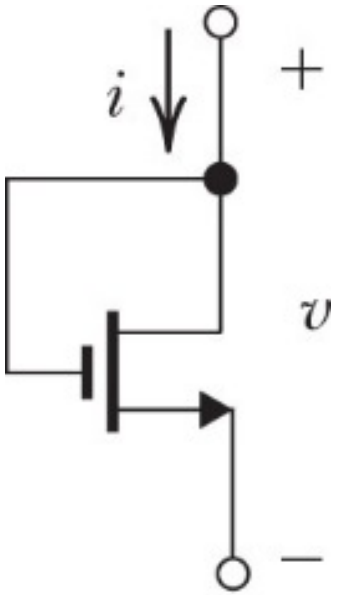


- **DC bias at Quiescent (Q) point**
- **Small-signal input superimposed on a DC bias voltage**
- **Symbol used in this course:**

$$v_{GS} = V_{GS} + v_{gs}$$

- **Need to know the transistor's I-V characteristics to find the voltage gain (and other properties of the amplifier)**

Diode-Connected Transistor



With Gate connected to Drain, it becomes a 2-terminal device.

This is called "diode-connected transistor"

In this configuration, the transistor is always in "Saturaiton".

Its I-V relationship is:

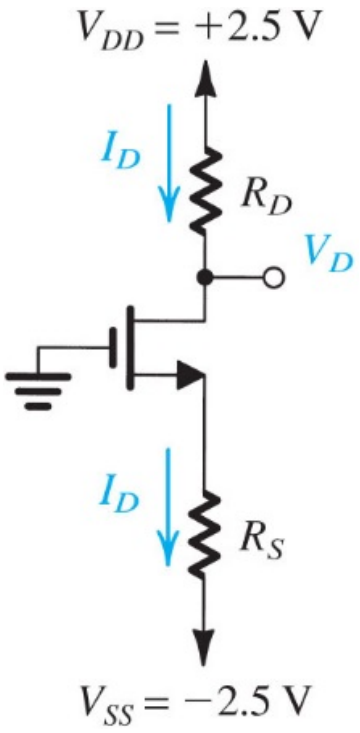
$$i = I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}v_{OV}^2$$

$$v_{GS} = v_{DS} = v$$

$$v_{OV} = v_{GS} - V_{tn} = v - V_{tn}$$

$$i = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(v - V_{tn}\right)^2$$

Example Circuit (1)



Design Problem:

Determine R_S and R_D such that the NMOS is biased at $I_D = 0.4mA$ and $V_D = 0.5V$. The NMOS has $V_t = 0.7V$, $\mu_n C_{ox} = 100\mu A/V^2$, $L = 1\mu m$ and W $= 32\mu m$.

Solution:

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{2.5 - 0.5}{0.4} = 5k\Omega$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}v_{OV}^2 = 0.4mA \text{ --> } v_{OV} = 0.5V$$

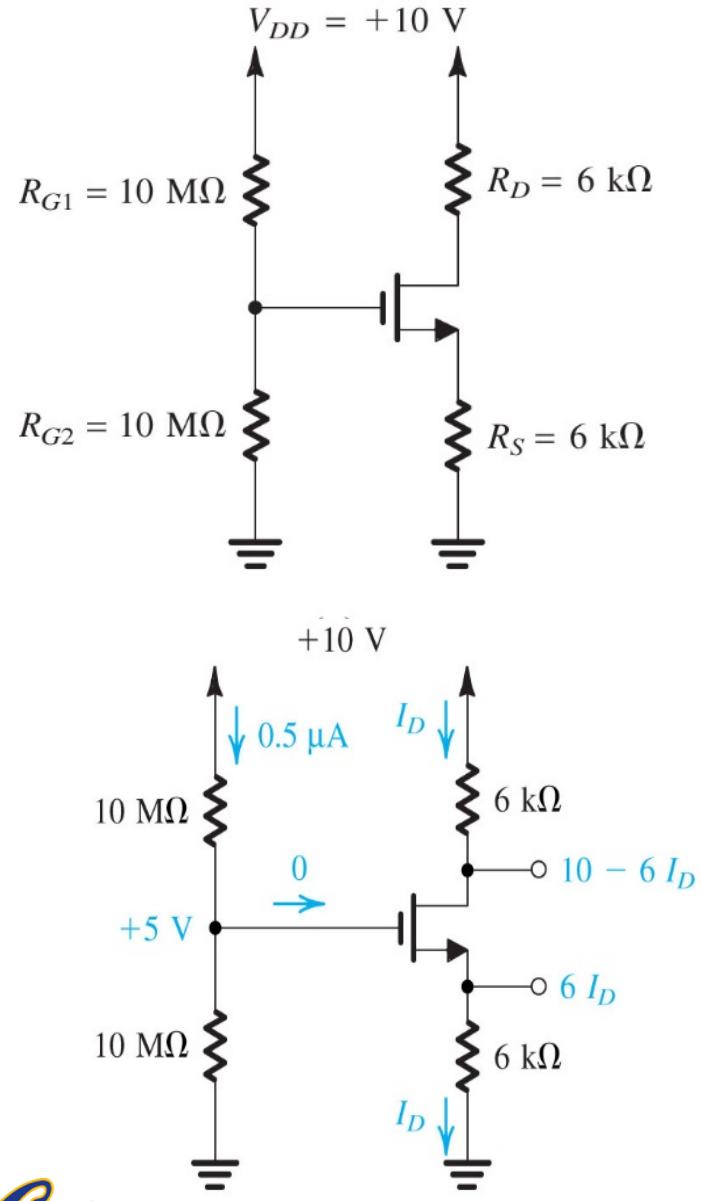
(channel length modulation can usually be ignored when solving DC bias)

$$v_{GS} = V_t + v_{OV} = 0.7 + 0.5 = 1.2V$$

$V_G = 0$ (grounded) --> $V_S = -1.2V$

$$R_D = \frac{V_S - V_{SS}}{I_D} = \frac{-1.2 - (-2.5)}{0.4} = 3.25k\Omega$$

Example Circuit (2)



The resistor divider is a common bias circuit.

To solve the DC bias condition, it means to solve I_D, V_{DS}, V_{GS}

The NMOS has $V_{tn} = 1V$, $k_n = \mu_n C_{ox} \frac{W}{L} = 1mA/V^2$

First, solve $V_G = V_{DD} \frac{R_{G2}}{R_{G1} + R_{G2}} = 10 \frac{5}{5+5} = 5V$

$V_{GS} = 5 - I_D R_S = 5 - 6I_D$ (with I_D in mA)

Next, assume the transistor is in saturation:

$$I_D = \frac{1}{2} k_n v_{OV}^2 = 0.5(V_{GS} - V_{tn})^2 = 0.5(5 - 6I_D - 1)^2$$

$18I_D^2 - 25I_D + 8 = 0$ --> $I_D = 0.89\text{mA}$ or 0.5mA

If $I_D = 0.89mA$, $V_{GS} = -0.34V$, NMOS will be cut-off

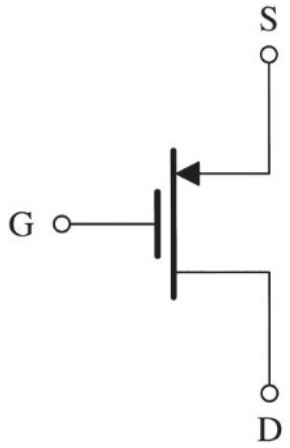
--> not a physical solution.

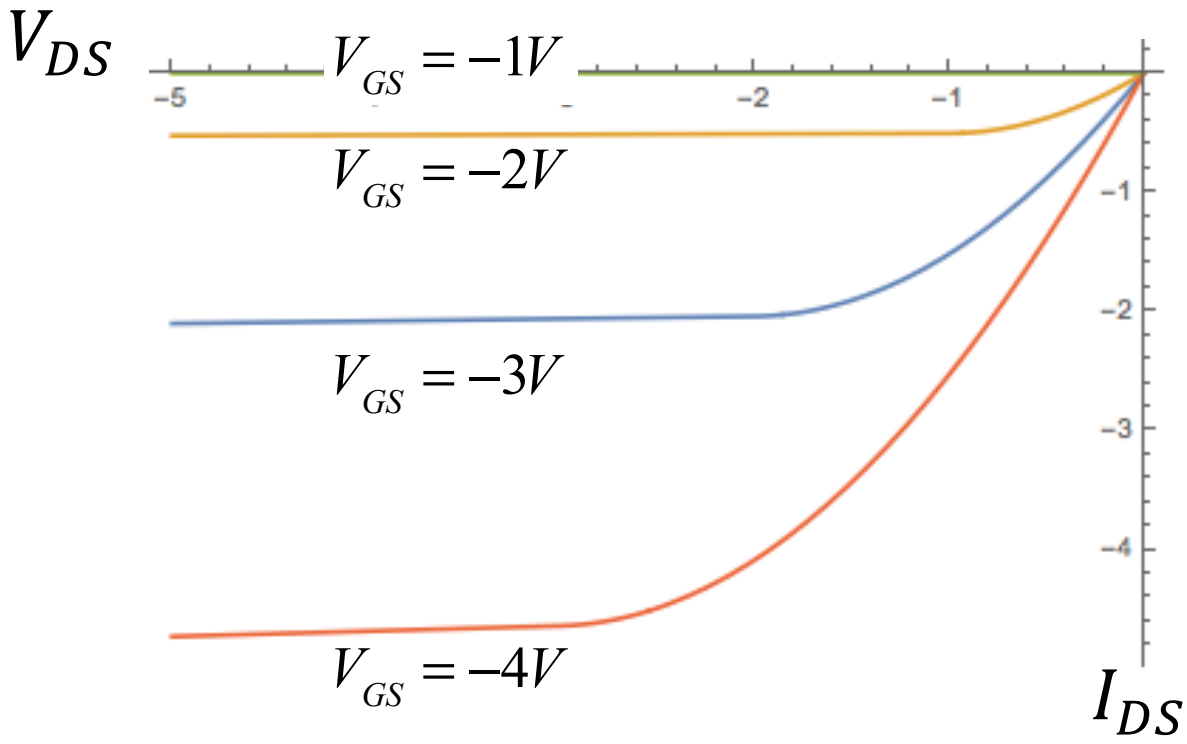
If $I_D = 0.5\text{mA}$, $V_{GS} = 2V$, $V_{OV} = 2 - 1 = 1V$

$V_{DS} = V_{DD} - I_D(R_D + R_S) = 10 - 6 = 4V > V_{OV}$

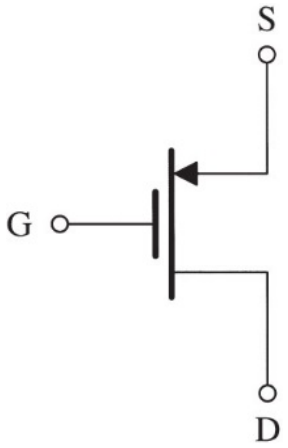
Saturation assumption verified !

PMOS I-V Curves

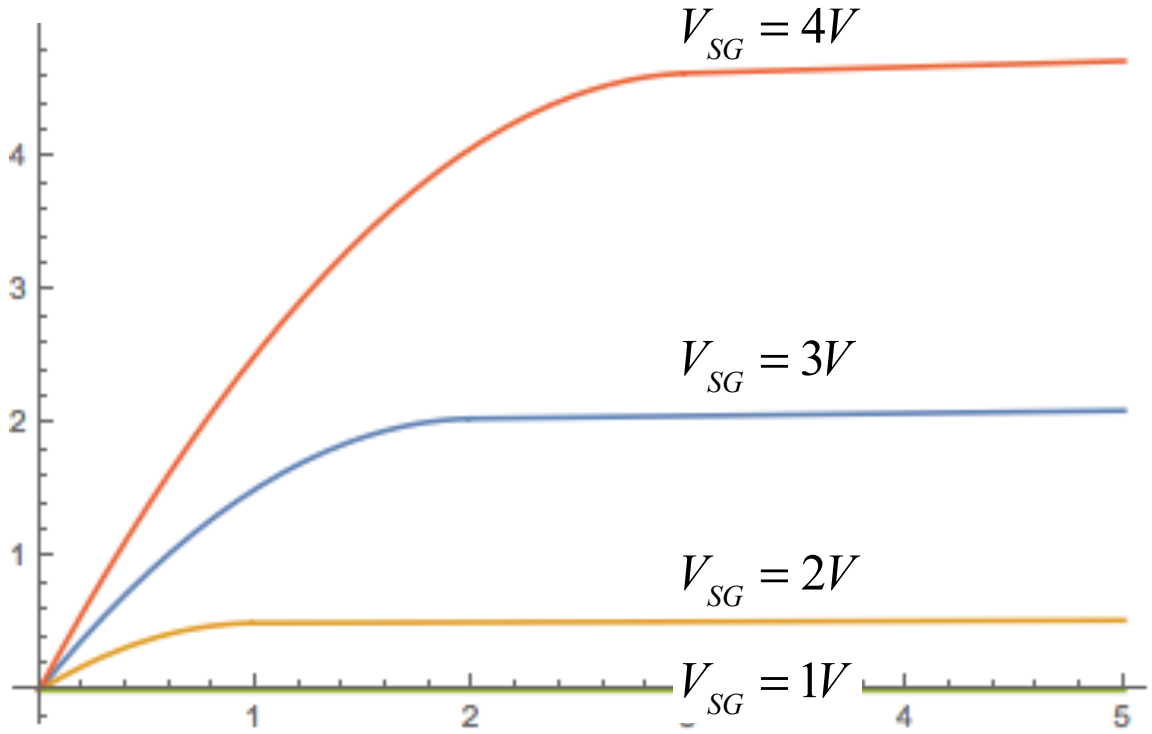




Right Side Up!

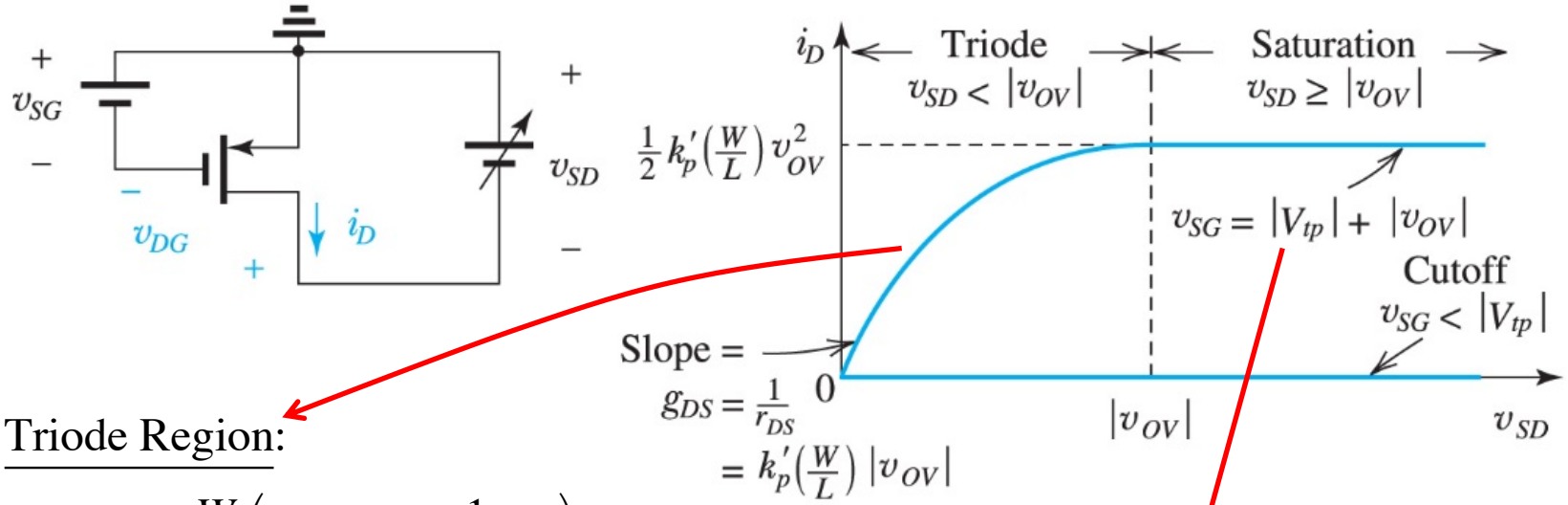


$$I_{SD} = |I_{DS}|$$



$$V_{SD} = |V_{DS}|$$

PMOS I-V Equations



Triode Region:

$$i_D = \mu_p C_{ox} \frac{W}{L}\left(|v_{OV}||v_{DS}| - \frac{1}{2}v_{DS}^2\right)$$

$$v_{OV} = |v_{SG}| - |V_{tp}|$$

Use same equation as NMOS but add absolute sign on all voltages since most voltages are negative:

$V_{tp} < 0,\ v_{DS} < 0,\ v_{GS} < 0$

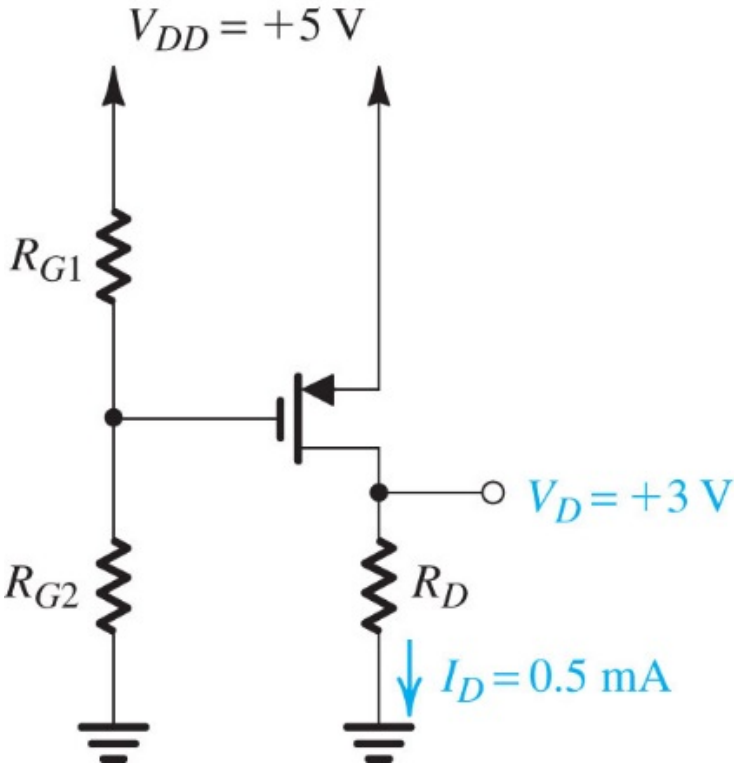
So either use v_{SD} or $|v_{DS}|$

Saturation Region:

$$i_D = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)\left(|v_{GS}| - |V_{tp}|\right)^2$$

$$= \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)v_{OV}^2$$

Example Circuit (3)



Design Problem:

Design the circuit such that $I_D = 0.5mA$ and $V_D = 3V$.

PMOS has $V_{tp} = -1V$, $\mu_p C_{ox}(W/L) = 1mA/V^2$.

Also find the maximum R_D for PMOS to remain in Saturation

Solution:

$$I_D = \frac{1}{2}k_p V_{OV}^2 = 0.5mA \text{ --> } |V_{OV}| = 1V$$

$$|V_{GS}| = |V_{tp}| + |V_{OV}| = 1 + 1 = 2V$$

$$V_S = 5V \text{ --> } V_G = 3V$$

We can choose $R_{G1} = 2M\Omega$ and $R_{G2} = 3M\Omega$

Saturation: $V_D \le 5 - |V_{OV}| = 4V$

$$R_{D,\max} = \frac{V_{D,\max}}{I_D} = \frac{4}{0.5} = 8k\Omega$$

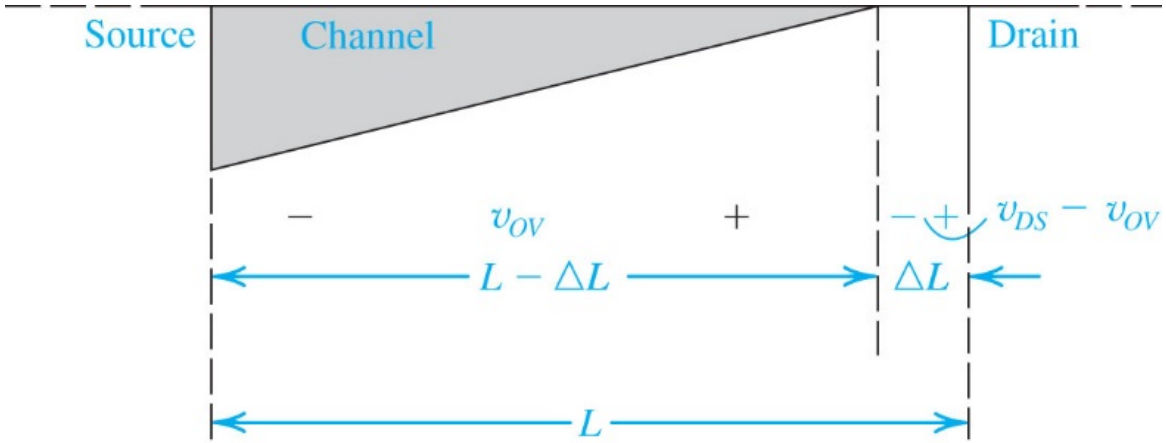
Finite Output Resistance due to Channel Length Modulation

When $v_{DS} = v_{OV}$, the channel pinch of near the Drain. With further increase in v_{DS}, the pinch off point moves slowly towards the source, effectively reducing the channel length from L to $L - \Delta L$ (this is called "channel length modulation"):

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L-\Delta L}\left(v_{GS} - V_{tn}\right)^2$$

The continual increase of i_D with v_{DS} is modeled by

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(v_{GS} - V_{tn}\right)^2\left(1 + \lambda v_{DS}\right)$$



Output Resistance of MOSFET

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(v_{GS}-V_{tn}\right)^2\left(1+\lambda v_{DS}\right)$$

$$r_o = \left(\frac{\partial v_{DS}}{\partial i_D}\right)_{v_{GS}=V_{GS}} = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}_{v_{GS}=V_{GS}} = \frac{1}{\lambda\left(\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS}-V_{tn}\right)^2\right)} \approx \frac{1}{\lambda I_D}$$

$$\boxed{r_o = \frac{1}{\lambda I_D}}$$ where $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS}-V_{tn}\right)^2$ is the DC bias current at Drain.